REMARKS

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by DeKoning et al. Claims 2-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over DeKoning et al. in view of Neufled. Reconsideration and withdrawal of the rejections of record are requested in view of the following discussion.

In the Action, at the second paragraph on page 2, the Examiner states, "it is noted that the features upon which applicant relies are not recited in the rejected claim(s)." Examiner then sets forth certain arguments presented by the applicant and concludes that: "Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims." In the quoted portion of applicant's argument, the only element set forth is the "host/network interface." However, all of applicant's claims set forth a host/network interface. See, for example, claim 1, element b). If the Examiner believes that applicant's argument has relied upon features which are not present in the claims, it is requested the Examiner specifically identify which argued features relied upon are not present in the claims.

In the third paragraph on page 2 of the Action, referencing applicant's contention that ". . . XOR 62 as taught by DeKoning et al. is not coupled to the host interface . . ." the Examiner sets forth reasons for the Examiner's disagreement with this contention which continues through the top of page 4. The essence of the Examiner's argument appears to be that DeKoning's memory controller (60) is analogous to the applicant's host/network interface. See the top of page 4 of the Action.

The Examiner further states in the Action, page 3, "The RPA memory controller 60 controls (1) the flow of data between the system bus 28, the RPA memory 22, and the intermediate parity buffer 64, and (2) the operation of the XOR engine 62." In response, applicant respectfully

submits that such functionality does not in any way correspond to the host/network interface of applicant's invention. In particular, as previously argued by applicant, at page 10 of applicant's prior response, applicant defines the host/network interface 31 as:

"a communications interface to a host computer or a network of computers. In one embodiment, the invention maintains an ANSI-X3T11 fiber channel interface utilizing a SCSI command set on the front end . . ."

In this connection, applicant is not suggesting that the host/network interface is an ANSI-X3T11 fiber channel interface utilizing an SCSI command set on the front end, but clearly such functionality is not in any way met by DeKoning's RPA memory controller 60 as that functionality is described by DeKoning and the Examiner. Thus, for the Examiner to conclude that the RPA memory controller 60 is equivalent to applicant's host/network interface 31 is simply not understood.

Additionally, in an attempt to explain to the Examiner the operational differences between DeKoning and the present invention, applicant notes the following.

As stated in the patent application on page 1 section [0011] "Since the XOR engine is placed in the data path and the parity is generated in real time during cache write transfers, the bandwidth overhead is reduced to zero." Relating this to DeKoning et al, in figure 2, the RPA memory (22) is equivalent to Applicant's central cache memory (35). The memory bus (66) in DeKoning et al is equivalent to Applicant's bus between XOR engine (31) and central cache memory (35). If we compare directly with a write request described in DeKoning starting in Column 5 line 46, DeKonings first chunk of data is transferred over the memory bus (66) and through the XOR engine (62) to the intermediate parity buffer (64) . Applicant's first chunk of data is transferred through the XOR Engine (31) and over the memory bus (between 31 and 35).

After transferring 4 chunks of data (column 6 line 35 in DeKoning et al.), DeKoning et al has 4 chunks of data in RPA Memory (22). After this same amount of time Applicant has 4 chunks of data in central cache memory (35) with its associated parity. DeKoning et al must now transfer parity data from the intermediate parity buffer (64) over the memory bus (66) into RPA memory (22). This step is described in DeKoning et al, column 6 lines 36-46. This is the step that Applicant does not perform because of the invented XOR placement. Applicant transfers the XOR data in parallel while calculating the XOR value in real time. This means Applicant does not need to perform the extra transfer over the memory bus, so there is no bandwidth overhead.

Note that the foregoing operational explanation is not intended to be considered as elements of applicant's claim, but is provided merely to assist the Examiner in obtaining an understanding of the invention, with the expectation that with such understanding, the Examiner will be in a better position to understand that the unique placement of the XOR engine in applicant's invention produces a result which is not possible based upon the teachings of DeKoning.

In view of the foregoing, reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 102(b) is requested.

Regarding the rejection of claims 2-13 under 35 U.S.C. § 103 over DeKoning et al. in view of Neufled, applicant submits that, since it has been demonstrated that DeKoning et al. does not teach the elements of applicant's claim 1, and since Neufled does not cure the deficiencies, applicant submits that claims 2-13 are patentably distinct over the prior art as well.

In view of the foregoing, reconsideration and withdrawal of the rejection of claims 1-13 is requested.

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Respectfully submitted,

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Dated: August 5, 2005

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Kenneth Schmidt — August 5, 2005